WE CLAIM

1. In a system comprising an interconnect and a plurality of modules connected to said interconnect for putting information onto the interconnect, a circuit comprising:

circuitry for receiving at least part of said of said information;

circuitry for determining if said at least part of said information satisfies one or more conditions; and

circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions.

2. A circuit as claimed in claim 1, wherein said action comprises the generation of a trace message.

3. A circuit as claimed in claim 1, wherein said action comprises the generation of an interrupt message.

4. A circuit as claimed in claim 3, wherein the interrupt is provided to one or more CPUs.

5. A circuit as claimed in claim 1, wherein said action is to prevent one or modules from being granted access to the interconnect.

6. A circuit as claimed in claim 5, wherein circuitry is provided to prevent one or more modules from being granted access to the interconnect.

7. A circuit as claimed in claim 6, wherein said circuitry for preventing a module from putting further information onto the interconnect comprises a register.

8. A circuit as claimed in claim 7, wherein the register comprises one bit for each module and the value of said

bit determines if the respective module is prevented from putting further information into the interconnect.

9. A circuit as claimed in claim 8, wherein at least one module is arranged to access said register non intrusively.

10. A circuit as claimed in claim 8, wherein a location is defined in said register for each module, the location being independent of the address of the module used by the interconnect.

11. A circuit as claimed in claim 6, wherein the module which puts the information onto the interconnect which matches the one or more conditions is prevented by the preventing circuitry from being granted access to the interconnect.

12. A circuit as claimed in claim 1, wherein the determining circuitry comprises comparator circuitry which compares the information on the interconnect with one or more match conditions.

13. A circuit as claimed in claim 1, wherein said conditions comprise one or more preconditions and one or more match conditions, said actions being performed when said one or more preconditions and said one or match conditions have been satisfied.

14. A circuit as claimed in claim 13, wherein one precondition is that the one or more match conditions have occurred a predetermined number of times.

15. A circuit as claimed in claim 13, wherein one precondition is that the circuit is enabled.

16. A circuit as claimed in claim 13, wherein one precondition is that circuitry external to said circuit has been enabled.

17. A circuit as claimed in claim 16, wherein said external circuitry is a latch.

18. A circuit as claimed in claim 13, wherein said match conditions comprise one or more of the following:
an address or address range of the information;
the module or modules which put the information onto the interconnect;
the module or modules which are intended to receive the information on the interconnect; and
the type or types of transaction to which the information relates.

19. A circuit as claimed in claim 1, wherein storing circuitry is provided to store the information which satisfies the at least one condition.

20. A circuit as claimed in claim 1, wherein said information comprises packets of information.

21. A circuit as claimed in claim 1, wherein said information comprises requests and responses.

22. A circuit comprising:
an interconnect;
one or more modules connected to the interconnect; and
a circuit for monitoring information put onto the interconnect by one or more modules, said circuit comprising:
circuitry for determining if the information on the interconnect matches one or more conditions; and
circuitry for performing one or more actions if it is determined that information on the interconnect matches said one or more conditions.

23. A circuit as claimed in claim 22, wherein the circuit is an integrated circuit.

24. A circuit as claimed in claim 22, wherein at least one module is external to said integrated circuit.

25. A circuit as claimed in claim 22, wherein an arbiter is provided for arbitrating between the modules to determine which module is granted access to the interconnect at a given time.

26. A circuit as claimed in claim 25, wherein said determining circuitry is at least partially in the arbiter.

27. A circuit as claimed in claim 25, wherein said determining circuit does not delay the arbitration provided by the arbiter.

28. A circuit as claimed in claim 22, wherein said interconnect is a bus.

29. A circuit as claimed in claim 22, wherein one of said modules comprises a debug module.

30. A circuit as claimed in claim 29, wherein at least some of said circuitry for performing at least one action is in said debug module.

31. A circuit as claimed in claim 25, wherein at least some of said circuitry for performing at least one action is in said arbiter.

32. A circuit as claimed in claim 29, wherein at least part of the determining circuitry is in the debug module.

33. A method comprising the steps of:
monitoring information on an interconnect, the information being put onto the interconnect by one or modules;

determining if the information on an interconnect satisfies one or more conditions; and

carrying out one or more actions if it is determined that the information satisfies one or more conditions.

34. A circuit for monitoring information on an interconnect, said information being put onto the interconnect by one or more modules connected to the interconnect, said circuit being arranged to determine if the information satisfies one or more conditions.

35. A circuit for monitoring information on an interconnect, said information being put onto the interconnect by one or more modules connected to the interconnect, said circuit being arranged to determine if the information satisfies one or more conditions and to select the information satisfying the one or more conditions